WHAT IS CLAIMED IS:

1. A receiving circuit for demodulating a received signal and detecting a synchronizing pattern from demodulated data in the demodulated received signal to thereby control the storage and output of desired data included in the demodulated data in response to the detected synchronizing pattern, comprising:

a demodulator circuit which demodulates the received signal and outputs the demodulated data therefrom;

a detector which detects a synchronizing pattern included in the demodulated data and outputs an instruction signal for providing instructions for the result of detection;

a pulse generator capable of receiving the instruction signal and outputting a pulse signal each time a predetermined time elapses since the reception of the instruction signal;

a control circuit which outputs control signals corresponding to at least either one of the instruction signal and the pulse signal; and

a clock generator which generates a clock signal for storing and outputting desired data included in the demodulated data in response to the control signal.

2. The receiving circuit as claimed in claim 1,

further including a pulse transfer control circuit which receives the pulse signal therein and controls the transfer of a signal corresponding to the pulse signal to said control circuit according to a mode signal.

3. The receiving circuit as claimed in claim 1, wherein said pulse generator comprises a counter which performs counting based on an operating clock signal used to operate said receiving circuit, and further including a clock transfer control circuit which receives the operating clock signal therein and controls the transfer of a signal corresponding to the operating clock signal to said pulse generator according to a mode signal.

4. The receiving circuit as claimed in claim 2, wherein said mode signal specifies a normal operating mode at a first voltage level and specifies a bit error rate measuring mode at a second voltage level different from the first voltage level, and said pulse transfer circuit restrains the transfer of a signal corresponding to the pulse signal to said control circuit when the mode signal is of the first voltage level and permits the transfer of the signal corresponding to the pulse signal to said control circuit when the mode signal is of the second voltage level.

5. The receiving circuit as claimed in claim 3,

wherein said mode signal specifies a normal operating mode at a first voltage level and specifies a bit error rate measuring mode at a second voltage level different from the first voltage level, and said clock transfer control circuit restrains the transfer of a signal corresponding to the operating clock signal to said pulse generator when the mode signal is of the first voltage level and permits the transfer of the signal corresponding to the operating clock signal to said pulse generator when the mode signal is of the second voltage level.